Application No.: 09/826,035 Docket No.: 21806-00123-US

REMARKS

Claims 1-20 are pending in the application.

The objection to the Declaration is noted. One of the inventors, Peter D. Lafauci has refused to execute the application. The circumstances surrounding this refusal are set forth in a Petition under 37 C.F.R. § 1.47 which was filed in connection with this application. Favorable consideration of the Petition, filed with the application by express mail on April 4, 2001, is requested.

Withdrawal of the objection to Fig. 4 as not containing the legend "Prior Art" is requested. There is no indication in the specification that the applicants intended Fig. 4 to be prior art. The specification indicates the contrary, specifically on page 9 thereof, where it is stated that Fig. 4 shows a computer system which can be used to implement the present invention. The verification test bench is implemented as computer executable instructions on the device shown. Accordingly, it is not considered appropriate to include the legend "Prior Art" with Fig. 4.

Withdrawal of the rejection to claims 2, 6, 7, 9, 11, 13, 14, 17 and 19, is requested. Claims 2 and 6 have been amended to make it clear that it is an external interface that is connected to the core.

Claims 11, 13, 14, 17 and 19 all appear to properly recited the use of an external interface connected to a core of a SOC (system on chip).

Withdrawal of the rejection to claims 1-20 under 35 U.S.C. § 102 as being anticipated by Devins et al. (U.S. Pat. No. 6,539,522) under 35 U.S.C. § 102(e) is requested. The present invention provides for an efficient and economical method and system for testing external interfaces of cores of an SOC. In order to efficiently test these interfaces, a mirror interface which is a copy or duplicate of the external interface undergoing verification is created. The mirror interface is attached to a bus functional model which essentially models the internal SOC and has a bus 109 and processor model 110 to emit CPU bus cycles. The bus cycles emulate the

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behavior of a processor without requiring significant computer resources to fully simulate an actual processor.

In carrying out the invention, the mirror interface is an exact duplicate of the external interface of the core and permits an exchange of data between the mirror interface and external interface of the core. Test stimuli are supplied to the external interface using the mirror interface. The mirror interface, which is a copy of the existing interface, avoids the need to develop a test model or a costly standardized model. The mirror interface provides for direct coupling with the external interface, as it has the same inputs and outputs of the external interface undergoing tests.

Turning now to the cited Devins et al. patent (U.S. Pat. No. 6,539,522), a method for developing reusable software for verifying SOC integrated circuit designs is disclosed. The system relies on hierarchical software, which has a partition between the upper-level test application code generating test cases and low level device driver codes for applying the test case to a hardware level. One embodiment disclosed in the reference provides a functional model to emulate various processor bus cycles, so that that testing can be speeded up over that provided by an embedded processor.

The reference does not appear to describe any mirror interface as is disclosed and claimed in the present application. The subject matter of Fig. 9, which the Office Action alleges illustrates a bus functional model which comprises a mirror interface (900) to the core, is mischaracterized. Item 900 of the reference refers in general to a bus functional module, not a mirror interface, which is used to drive signals to components of the simulated design avoiding the excessive processor time that a embedded processor represents. Further, there does not appear to be any handshake protocol operating between the simulated design and the mirror interface as is required by claim 1, to provide an exchange of data between the mirror interface and external interface. The bidirectional nature of the mirror interfaces as set forth in claims 3, 4 and 5 does not appear to be disclosed in the reference.

Claim 6 makes it clear that the mirror interface is a copy of the core which is not disclosed in the reference.

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Each of the remaining claims in the application requires use, or connection to, a mirror interface. As it has been set forth above, it is not seen where any such mirror interface is disclosed in the cited reference.

Further, it should be noted that claims 18-20 require various control features for controlling the mirror interface. A review of the cited reference fails to disclose any of these features as well.

In view of the foregoing, where it is seen that the cited reference does not disclose or suggest the claimed subject matter of the present application, favorable reconsideration is believed to be in order.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 22-0185, from which the undersigned is authorized to draw.

Dated: 9/3/03

Respectfully submitted,

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